REMARKS

Claims 88-123 are presently pending in this application, with claim 88 being the sole independent claim. Claim 89 has been cancelled, and its subject matter incorporated into claim 88. Thus, claims 88 and 90-123 are presently pending in the application. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**" Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

Claim 122 stands rejected under 35 U.S.C. § 112, fourth paragraph, for failing to further limit claim 121. This objection is respectfully traversed. Claim 121 recites an act of providing an insulating layer. Claim 122 recites an act of processing that insulating layer to produce an active circuit element. Since claim 122 recites the processing of the insulating layer of claim 121, it further limits the subject matter of claim 121.

In a telephone conference with the Examiner on October 16, 2001, the Examiner asserted that claim 122 is also redundant over claim 88 because both recite processing an insulating layer to produce a circuit element. However, claim 122 recites processing an insulating layer to produce an *active* circuit element, while claim 88 recites processing an insulating layer to produce a *passive* circuit element. Accordingly, claim 122 is not redundant over claim 88 and is in compliance with 35 U.S.C. § 112, fourth paragraph so that the rejection should now be withdrawn.

Claims 88-100, 105-118 and 123 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,770,476 to Stone ("Stone") in view of U.S. Patent No. 6,201,287 B1 to Forbes ("Forbes"). Reconsideration is respectfully requested.

As evidenced by the "Statement of Common Ownership" (attached), the present Application, numbered 09/660,324, and U.S. Patent No. 6,201,287 B1 (Forbes) describe and claim subject matter which, at the time the invention of Application 09/660,324 was

made, was commonly owned by Micron Technology Inc., Boise ID. For this reason, the Forbes reference is not available for use in a rejection of the present application. See M.P.E.P. §706.02(l)(2)II. Additionally, claim 88 has been amended to incorporate the subject matter of claim 89, and claim 89 has been cancelled.

The amended claim 88 now recites ". . . at least one integrated circuit chip is electrically connected to said at least one passive circuit element." The Office Action stated this feature can be found within Stone's Figure 2 (page 3, paragraph 4). Fig. 2 is described as showing an interposer 100 with an electronic devices 31, 33 joined on either side (col. 8, lines 31-36). Separately, Stone contemplates forming passive electronic components within the interposer layer 100. However, nowhere within the Stone reference, and certainly not within Figure 2, does Stone disclose an integrated circuit chip being electrically connected to a passive circuit element formed within an interposer layer, as claimed. Additionally, as stated by the Examiner, Stone does not show an insulating layer provided on a silicon substrate wherein a passive circuit element is separated from that silicon substrate by a portion of the insulating layer (page 3, paragraph 1). For at least the above reasons, the rejection of claim 88 and all claims dependent therefrom should now be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is

respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: October 26, 2001

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 828-2232
Attorneys for Applicant

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

88 (amended) A process for forming an interposer element for use as a chip carrier comprising the steps of:

providing an insulating layer on at least one surface of a silicon substrate; and

processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate,

bonding at least one integrated circuit chip to said interposer element such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element.

89. (cancel without disclaimer or prejudice)